S.E.(COMPUTER)(Sem III) (Choice Based) / 50902 - DIGITAL LOGIC DESIGN AND ANALYSIS

Duration: - 3 Hours Marks: 80 Marks

NB: - Question 1 is compulsory

Solve any three questions from the remaining.

1 a) Convert decimal number 576.24 into binary, base-9, octal, hexadecimal system. 04

b) Construct hamming code for 1010 using odd parity. 04

c) Convert $(-89)_{10}$ to its equivalent Sign Magnitude, 1's Complement and 2's Complement Form 04

d) Perform $(BC5)_H - (A2B)_H$ without converting to any other base 04

e) Prove De Morgans theorem 04

2a. Given the logic expression: $A + \overline{B}\overline{C} + AB\overline{D} + ABCD$ 10

1. Express it in standard SOP form.
2). Draw K-map and simplify.
3). Draw logic diagram using NOR gates only.

2b. Reduce using Quine McClusky method & realize the operation using only NAND gates. 10

$F(A,B,C,D) = \prod M(0,2,3,6,7,8,9,12,13)$.

3a. Design a 4-bit binary to gray code converter. 10

3b. Design a 4-bit BCD adder using IC 7483 and necessary gates. 10

4a. Implement the following logic function using all 4:1 multiplexers with the select inputs as 'B', 'C', 'D', 'E' only. 10

$F(A,B,C,D,E) = \sum m\ (0,1,2,3,6,8,9,10,13,15,17,20,24,30)$

4b. Convert a SR flip flop to J K flip flop 10

5a. Design a mod-6 synchronous counter using T FF 10

5b. Explain the operation of 4-bit universal shift register. 10

6 Write short notes on any two 20

a. VHDL
b. TTL and CMOS logic families
c. 4-bit Magnitude comparator
d. 3 to 8 line decoder
