

University of Mumbai
Examination 2020 under cluster 4 (PCE)

Program: TE Information Technology

Curriculum Scheme: Rev 2012

Examination: Third Year Semester V

Course Code: TEITC503 and Course Name: Microcontroller and Embedded Systems(MES)

Time: 1 hour

Max. Marks: 50

NOTE to the Question Bank Generator:

1. The question bank consists of 25 MCQ questions with each question carrying a maximum of 2 marks. It should cover all the modules with appropriate weightages.
2. You need to check the questions and their answers for their correctness. There should not be any ambiguity in the questions and the options. Only one option should be the Correct Answer.
3. You must ensure that the same question is not repeated again in this question paper.
4. Among 25-questions, 13 questions can be under the 'Simple' category, 7-questions can be under the 'Moderate' category, and the remaining 5-questions can be under the 'Difficult' category.
5. Please do not reveal answer on this Question Paper.
6. Use another template provided to enter the correct answers.
7. Please save this file with file name as per the sample format given below:

File Name: "Date of Examination_Scheme_Program_Semester_Subject Code_QP Set Number"

For example:

QP set number 1 of first core course of Mechanical Engineering Semester V for Rev2016 scheme and scheduled on 25/09/2020 has to have the file name as

2509_R16_Mech_V_MEC501_QP1

QP set number 1 of Department Level Optional Course of Computer Engineering Semester VI for Rev2012 scheme and scheduled on 28/09/2020 has to have the file name as

2809_R12_Comp_VI_CSDLO6021_QP3

Note to the students:- All the Questions are compulsory and carry equal marks .

Q1.	Which of the following offers external chips for memory and peripheral interface circuits?
Option A:	Microcontroller
Option B:	Microprocessor
Option C:	Peripheral system
Option D:	Embedded system
Q2.	Limited User Interface, small size, less cost and less power consumption are the specialities of ----- systems
Option A:	closed
Option B:	operating

University of Mumbai
Examination 2020 under cluster 4 (PCE)

Option C:	embedded
Option D:	computing
Q3.	Abbreviate CISC and RISC.
Option A:	Complete Instruction Set Computer, Reduced Instruction Set Computer
Option B:	Complex Instruction Set Computer, Reduced Instruction Set Computer
Option C:	Complex Instruction Set Computer, Reliable Instruction Set Computer
Option D:	Complete Instruction Set Computer, Reliable Instruction Set Computer
Q4.	PSEN stands for
Option A:	Program Select Enable
Option B:	Peripheral Store Enable
Option C:	Program Store Enable
Option D:	Peripheral Select Enable
Q5.	What is the operation for mode 1?
Option A:	13-bit timer mode, 8-bit timer/counter THx and TLx as 5-bit prescaler
Option B:	16-bit timer mode, 16-bit timer/counter THx and TLx are cascaded, no prescaler
Option C:	8-bit auto reload mode, 8-bit auto reload time/counter; THx holds a value which is to be reloaded into TLx each time it overflows
Option D:	Spilt timer mode
Q6.	What ROM location is reserved for external interrupt 1 (INT1)
Option A:	0003H
Option B:	001BH
Option C:	0013H
Option D:	000BH
Q7.	What is the address range of SFR Register bank?
Option A:	a) 00H-77H
Option B:	b) 40H-80H
Option C:	c) 80H-7FH
Option D:	d) 80H-FFH

University of Mumbai
Examination 2020 under cluster 4 (PCE)

Q8.	In 8051 MOV IE,# 1000 1000B instruction
Option A:	enable Timer 1 interrupt and disable Timer 0 interrupt
Option B:	enable Timer 0 interrupt and disable Timer 1 interrupt
Option C:	Enable both timer 1 and timer2 interrupt
Option D:	disable both timer 1 and timer2 interrupt
Q9.	In 8051 the conditional branching instructions specify the destination address by
Option A:	Relative offset method
Option B:	Absolute address method
Option C:	Either relative or absolute address method
Option D:	Complete 16 bit address
Q10.	one of the software tool running on IBM PC translate program written in C language for microcontroller to machine language of 8051, what is that software tool?
Option A:	Complier
Option B:	Cross complier
Option C:	Assembler
Option D:	Cross Assembler
Q11.	Which instruction is used in 8051 to terminate the Interrupt service routine (ISR).
Option A:	RET
Option B:	SJMP\$
Option C:	RETI
Option D:	LJMP
Q12.	Following is the assembler directive
Option A:	MOV A,B
Option B:	SWAP
Option C:	ORG
Option D:	SWAP
Q13.	An instruction that is used to move data from an ARM Register to a Status Register (CPSR or SPSR) is called _____.
Option A:	MRC
Option B:	MRS
Option C:	MSR
Option D:	MCS

University of Mumbai
Examination 2020 under cluster 4 (PCE)

Q14.	_____ is used for compare negative two 32-bit integer.
Option A:	LSL
Option B:	ASL
Option C:	CMN
Option D:	CMP
Q15.	In ARM Processor,when ORR instruction followed by MVN is effectively equal to
Option A:	NAND
Option B:	X-OR
Option C:	X-NOR
Option D:	NOR
Q16.	Which one of the following control signal could be used in the Execution stage of an instruction?
Option A:	MemRead
Option B:	RegWrite
Option C:	ALUop
Option D:	PCsrc
Q17.	In ARM Processor, SBC is used to_____
Option A:	To substract 8 bit numbers
Option B:	To substract 16 bit numbers
Option C:	To substract 32 bit number
Option D:	To substract 64 bit number
Q18.	Which of the following defines the set of instructions loaded into the memory?
Option A:	process
Option B:	task
Option C:	thread
Option D:	system hardware
Q19.	What is the main purpose of the memory management unit?
Option A:	address translation
Option B:	large storage
Option C:	reduce the size
Option D:	provides address space

University of Mumbai
Examination 2020 under cluster 4 (PCE)

Q20.	How is the number of chips required is determined?
Option A:	number of data lines
Option B:	the minimum number of data
Option C:	width of the data path from the processor
Option D:	number of data lines and the width of the data path from the processor
Q21.	Which of the following technique is used by the UNIX operating system?
Option A:	logical address memory
Option B:	physical address memory
Option C:	virtual memory technique
Option D:	translational address
Q22.	In which of the exceptions does the external event causes the exception?
Option A:	synchronous exception
Option B:	asynchronous exception
Option C:	precise
Option D:	imprecise
Q23.	_____ is a chip inside digital camera and its job is to classify the voltages of the pixels into levels of brightness and to assign each level to a binary number, consisting of zeros and ones.
Option A:	LCD
Option B:	Microcontroller
Option C:	ADC
Option D:	Sensor
Q24.	LCD stands for _____.
Option A:	Logical Crystalline Display
Option B:	Logical Crystal Display
Option C:	Liquid Crystalline Display
Option D:	Liquid Crystal Display
Q25.	The interface between an analog signal and a digital processor is _____.
Option A:	D/A converter
Option B:	Demodulator
Option C:	Modulator

University of Mumbai
Examination 2020 under cluster 4 (PCE)

Option D:	A/D converter

University of Mumbai
Examination 2020 under cluster 4 (PCE)

Program: TE Information Technology

Curriculum Scheme: Rev 2012

Examination: Third Year Semester V

Course Code: TEITC503 and Course Name: Microcontroller and Embedded Systems(MES)

Time: 1 hour

Max. Marks: 50

=====

NOTE: Please save this file with file name as per the sample format given below:

File Name:

Date of Examination_Scheme_Program_Semester_Subject Code_Answer Key Set Number

For example:

Answer Keys for QP set number 1 of first core course of Mechanical Engineering

Semester V for Rev2016 scheme and scheduled on 25/09/2020 has to have the file name as

2509_R16_Mech_V_MEC501_AK1

Answer Keys for QP set number 1 of Department Level Optional Course of Computer

Engineering Semester VI for Rev2012 scheme and scheduled on 28/09/2020 has to have

the file name as

2809_R12_Comp_VI_CSDLO6021_AK3

=====

Question	Correct Option (Enter either 'A' or 'B' or 'C' or 'D')
Q1.	B
Q2.	C
Q3.	B
Q4	C
Q5	B
Q6	C
Q7	D
Q8.	A
Q9.	A
Q10.	D
Q11.	C
Q12.	C
Q13.	C
Q14.	C
Q15.	D
Q16.	C
Q17.	D
Q18.	B
Q19.	A
Q20.	B
Q21.	C
Q22.	B
Q23.	C

University of Mumbai
Examination 2020 under cluster 4 (PCE)

Q24.	D
Q25.	D