University of Mumbai

Examination 2020 under cluster 4 (PCE)

Program: Computer Engineering
Curriculum Scheme: Rev2016
Examination: Third Year Semester V
Course Code: CSC501 and Course Name: Microprocessor

Time: 1 hour Max. Marks: 50

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Note to the students:- All the Questions are compulsory and carry equal marks .

Q1.	In fetch-decode unit, the number of parallel decoders that accept the stream of fetched instructions and decode them is
Option A:	1
Option B:	2
Option C:	3
Option D:	4
Q2.	The common register(s) for all the four channels of 8257 is
Option A:	DMA address register
Option B:	Terminal count register
Option C:	Mode set register and status register
Option D:	None of the mentioned
Q3.	A 5 stage pipeline with the stages taking 1, 1, 3, 2, 1 units of time has throughput of
Option A:	1/3
Option B:	1/5
Option C:	1/7
Option D:	1/8
Q4.	In instruction issue algorithm which of the following condition are true the two instruction(I1 &I2) are pairable. a) I1 &I2 instruction are simple. b)1 is not jump instruction. c) Destination of I1is not the source of I2. d)Destination of I1is not the Destination of I2. e) Destination of I2is not the source of I1.
Option A:	abcd
Option B:	bcde
Option C:	acde
Option D:	abde
Q5.	Which following cases write back occurs in burst bus cycle of Pentium processor
Option A:	External and Internal snoop hit to modified line and modified line to be replaced.
Option B:	External and Internal snoop hit to un-modified line and un-modified line to be replaced.
Option C:	External and Internal snoop hit to un-modified line and un-modified line to be added.

Option D:	External and Internal snoop hit to modified line and modified line to be added.
Q6.	The area of memory from the start of the second segment to the possible end of the first segment is called an _____ segment area.
Option A:	Primary
Option B:	Overlapped
Option C:	Separate
Option D:	Secondary
Q7.	The BIU fetches _____instruction bytes in a single memory cycle.
Option A:	One
Option B:	Two
Option C:	Four
Option D:	Six
Q8.	When the 8086 is set for the _____mode configuration, it provides signals for implementing a multiprocessor / coprocessor system environment.
Option A:	Minimum
Option B:	Maximum
Option C:	I/O
Option D:	Memory
Q9.	_____ interrupt can be disabled by making IF=0.
Option A:	NMI
Option B:	INTR
Option C:	INT21H
Option D:	INT 10H
Q10.	Advantage of segmentation is it permits the programmer to access 1MB memory using ___ bit address.
Option A:	4
Option B:	8
Option C:	16
Option D:	32
Q11.	Active low BHE pin of 8086 microprocessor is used to interface the
Option A:	Even bank memory
Option B:	Odd bank memory
Option C:	I/O
Option D:	DMA
Q12.	_____ register is used to hold the first operand and the result in complex arithmetic operations like Multiply and Divide.
Option A:	IP
Option B:	CS
Option C:	AX
Option D:	CX

Q13.	The instruction that is not possible among the following is
Option A:	MOV AX, [BX].
Option B:	MOV AX, 5555H
Option C:	MOV AX, [SI].
Option D:	MOV [SI], [DI].
Q14.	The extension that is essential for every assembly level program is
Option A:	.ASP
Option B:	.ALP
Option C:	.ASM
Option D:	.PGM
Q15.	DEBUG is able to troubleshoot only
Option A:	.EXE files
Option B:	.OBJ files
Option C:	.EXE file and .OBJ file
Option D:	.EXE flie and .LST file
Q16.	When a stack segment is initialised then
Option A:	SS and SP are initialised
Option B:	only SS is initialised
Option C:	only SP is initialised
Option D:	SS and SP need not be initialised
Q17.	8086 does not support
Option A:	Arithmetic operations
Option B:	logical operations
Option C:	BCD operations
Option D:	Direct BCD packed multiplication
Q18.	For 8086 microprocessor, the stack segment may have a memory block of a maximum of
Option A:	32K bytes
Option B:	64K bytes
Option C:	16K bytes
Option D:	NONE
Q19.	In the instruction, ASSUME CS : CODE, DS : DATA, SS : STACK the ASSUME directive directs to the assembler the
Option A:	address of the stack segment
Option B:	pointer address of the stack segment
Option C:	name of the stack segment
Option D:	name of the stack, code and data segments
Q20.	In the application where all the interrupting devices are of equal priority, the

	mode used is
Option A:	Automatic Rotation mode
Option B:	EOI Mode
Option C:	Specific Rotation mode
Option D:	Automatic EOI mode
Q21.	The register that stores the bits required to mask the interrupt inputs is
Option A:	Interrupt Service Register
Option B:	Interrupt Mask Register
Option C:	Interrupt Request Register
Option D:	Priority Resolver
Q22.	_____ locations are reserved for interrupt vector table.
Option A:	00000-07FFFH
Option B:	00000-003FFH
Option C:	00000-FFFFFH
Option D:	FFFF0-FFFFFH
Q23.	Name the default mode of 8259.
Option A:	Special Mask Mode
Option B:	Special fully nested mode
Option C:	Fully nested mode
Option D:	EOI Mode
Q24.	when OCW1 is sent to 8259
Option A:	To set priority of interrupts
Option B:	to decide cascading is needed or not
Option C:	To mask or unmask interrupts
Option D:	To set in Default mode
Q25.	When of following statment is FALSE reg ICW4
Option A:	ICW4 is required when we want to work with 8086
Option B:	When we want to set Buffered Mode
Option C:	When we want to set Auto EOI
Option D:	when we want to pass vector address to Microprocessor

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Question	Correct Option (Enter either 'A' or 'B' or 'C' or 'D')
Q1.	B
Q2.	C
Q3.	D
Q4	A
Q5	A
Q6	B
Q7	B
Q8.	B
Q9.	B
Q10.	C
Q11.	B
Q12.	C
Q13.	D
Q14.	C
Q15.	A
Q16.	A
Q17.	D
Q18.	B
Q19.	D
Q20.	A
Q21.	B
Q22.	C
Q23.	C
Q24.	C
Q25.	D