Time : 3 Hours **Max Marks: 80**

1. Question No. 1 is compulsory.
2. Out of remaining questions, attempt any three questions.
3. Assume suitable additional data if required.
4. Figures in brackets on the right hand side indicate full marks.

1. (A) Compare PAL and PLA. (05)
   (B) Define the following terms of Logic Families: (05)
   (i) Power Dissipation
   (ii) Figure of Merit
   (C) Prove the following using Boolean Algebra (05)
   $$AB + \bar{A}C = (A + C)(\bar{A} + B)$$
   (D) Compare Synchronous counter with Asynchronous counter. (05)

2. (A) Design synchronous counter using T-type flip flops for getting the following sequence: $1 \rightarrow 3 \rightarrow 5 \rightarrow 7 \rightarrow 1$ (10)
   Take care of lockout condition.
   (B) Perform $(28)_{10} - (52)_{10}$ operation using 2's compliment method. (05)
   (C) Write $(32)_8$ into its Binary code, BCD code, and Hexadecimal code. (05)

3. (A) Implement the following Boolean equation using single 4:1 MUX and few logic gates: (10)
   $$F(P,Q,R,S) = \Pi M(0, 2, 5, 6, 7, 9, 12, 15)$$
   (B) Compare Combinational circuits with Sequential circuits. (05)
   (C) Implement a circuit having two inputs *A* and *B* and single output *Y* such that for any inputs of *A* and *B*, the output *Y* will always be 1 (i. e. $Y = 1$) using only NAND gates. (05)

4. (A) Draw a neat circuit of BCD adder using IC 7483 and explain. (10)
   (B) Using Quine McClusky method, minimize the following: (10)
   $$F(P,Q,R,S) = \sum m(1, 2, 3, 5, 9, 12, 14, 15) + d(4, 8, 11).$$

5. (A) Write VHDL code for negative edge triggered 3 bit binary down counter with active low Preset and Clear terminal. (10)
   (B) Convert JK type flip flop into D type flip flop. (05)
   (C) Compare SRAM with DRAM. (05)

6. (A) What is shift register? Explain any one type of shift register. Give its application. (10)
   (B) Design a Mealy type sequence detector circuit to detect a sequence 1101 using T type flip flops. (10)

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