B.E. (Biomedical) (REV. -2012)(CBSGS) SEMESTER -VII / 41704 - Very Large Scale Integrated Circuits

Q.P. Code : 40423

[Time: 3 Hours]　　　　　　　　　　　　　　　　　　　　　[Marks: 80]

Please check whether you have got the right question paper.

N.B:　1. Questions **1** is **compulsory.**
　　　2. Attempt any **three** out of remaining **five.**
　　　3. State your Assumptions.
　　　4. Use graph sheet for layout.

1. (a) Explain oxidation process in IC fabrication.　　　　　　　　　　5
   (b) Explain basic structure of VHDL.　　　　　　　　　　　　　5
   (c) Draw the transfer characteristics of CMOS inverter and define Noise　5
   Margin.
   (d) Explain voltage current relationship in N-MOS transistor under　　5
   various operating condition.

2. (a) Explain the architecture of FPGA XC-4000 series with block　　10
   diagrams.
   (b) Find the depletion layer width x_d , the depletion region charge Q_{BO} ,　10
   the threshold voltage with no source to Body voltage V_{THO} , of a
   MOS transistor with the following parameters. $t_{ox} = 400^0 A$,
   N_a (substrate doping density)$= 1.5 \times 10^{16}/cm^3$, N_D (gate donor doping)
   $= 10^{18} /cm^3$, N_{ox} (oxide interface charge) $= 5 \times 10^{10}/cm^2$, $\varepsilon_{ox} = 3.97$
   ε_o ; $\varepsilon_{si} = 11.7 \varepsilon_o$; $\varepsilon_o = 8.854 \times 10^{-14}$ F/cm

3. (a) Write VHDL code for 3:8 decoder using any one modeling　　4
   techniques.
   (b) Write VHDL code for 1 bit full adder using half adder as components　6
   (c) Explain briefly various MOS capacitance　　　　　　　　　6
   (d) Write short channel effect in MOSFET　　　　　　　　　4

4. (a) Explain the complete fabrication process steps for a CMOS inverter　　10
   using P-well process with the help cross sectional diagrams for all
   important masking steps.
   (b) Derive the expression for V_{IL} , V_{IH} , V_{OH} , V_{OL} , for the depletion load　　10
   n-MOS inverter in terms of device parameters.

5. (a) Draw λ- based layout for 2 input NOR gate with depletion MOSFET   10
       as load. With aspect ratio (L/W) for load is 2:1 and drivers is 1:2

   (b) Distinguish between full scaling and constant voltage scaling.   10

6. (a) Draw the circuit diagram and stick diagram for the given expression   5
       F = A⊕B using N-MOS Depletion load

   (b) Write a short note on Butt and Buried contact   7

   (c) Write a short note on Latch up problem in CMOS and ways to   8
       minimize it.