University of Mumbai

Examination 2020

Program: BE Biomedical Engineering
Curriculum Scheme: Rev2016
Examination: Fourth Year Semester VII

Course Code: **BMC702** and Course Name: **Basics of VLSI**

Time: 1 hour Max. Marks: 50

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Note to the students: - All the Questions are compulsory and carry equal marks .

Q1.	What is not a part of VHDL Code?
Option A:	Library declaration
Option B:	Entity declaration
Option C:	Architecture
Option D:	Logic family
Q2.	By which Statement a new data type can be included in VHDL?
Option A:	Type
Option B:	If
Option C:	Process
Option D:	std_logic
Q3.	Behavioral coding style is compulsory for ----- circuits
Option A:	data
Option B:	combinational
Option C:	analog
Option D:	sequential
Q4.	Name VHDL Library where logic functions are described-
Option A:	IEEE.STD_LOGIC_1164.ALL
Option B:	IEEE.STD_LOGIC_ARITH.ALL
Option C:	IEEE.STD_LOGIC_UNSIGNED.ALL
Option D:	There is no library where logic functions are described
Q5.	Assignment statement for signal declaration is -
Option A:	y=:"1001"
Option B:	y:="0001"
Option C:	y<="0001"
Option D:	y=0001
Q6.	In what way the instructions are executed in the 'Process' statement of VHDL Code?
Option A:	Sequentially
Option B:	Concurrently
Option C:	Boolean
Option D:	std_logic

Q7.	which of the following statement will not come in any style of VHDL Code for 3 line to 8 line decoder?
Option A:	Process statement
Option B:	when statement
Option C:	if clock' event and clock='1' then
Option D:	If Statement
Q8.	In nMOSFET the majority carriers of substrate are:
Option A:	Holes
Option B:	Negative ions
Option C:	Electrons
Option D:	positive ions
Q9.	Surface mobility depends on -
Option A:	effective drain voltage
Option B:	effective gate voltage
Option C:	channel length
Option D:	effective source voltage
Q10.	In MOSFET, Transconductance gives the relationship between _____
Option A:	input current and output voltage
Option B:	output current and input voltage
Option C:	input current and input voltage
Option D:	output current and output voltage
Q11.	High level Noise Margin of inverter is-
Option A:	VIL~VOL
Option B:	VIH~VOH
Option C:	VIH~VOL
Option D:	VIL~VIH
Q12.	When Vin<Vto driver transistor will be in-
Option A:	Cut off region
Option B:	Saturation region
Option C:	Linear region
Option D:	Can't say
Q13.	When input voltage is V_{IL} the operating region of driver transistor in depletion load NMOS inverter is-
Option A:	Cut off region
Option B:	Saturation region
Option C:	Linear region
Option D:	Can't say
Q14.	Which of the following is not due to small geometry effects?
Option A:	Short channel effect
Option B:	Punch through
Option C:	Hot carrier effect

Option D:	Channel length modulation
Q15.	When input voltage is VIH the operating region of PMOS transistor in CMOS inverter is-
Option A:	Cut off region
Option B:	Saturation region
Option C:	Linear region
Option D:	Threshold region
Q16.	In CMOS Inverter PMOS acts as-
Option A:	LOAD
Option B:	Driver
Option C:	Pull down
Option D:	Short to ground
Q17.	What type of light source is used for patterning the photoresist layer in CMOS fabrication?
Option A:	visible light
Option B:	ultraviolet light
Option C:	infrared light
Option D:	Fluorescent
Q18.	What is used for the fabrication of nMOS?
Option A:	thin wafer of a single crystal
Option B:	thin wafer of multiple crystals
Option C:	thick wafer of a single crystal
Option D:	thick wafer of multiple crystals
Q19.	On which layer contact cuts are made?
Option A:	Source
Option B:	Substrate
Option C:	metal layer
Option D:	diffusion layer
Q20.	What is responsible for the 'Latch – up' problem?
Option A:	Parasitic R
Option B:	Parasitic BJT's
Option C:	(A) & (B)
Option D:	Parasitic C
Q21.	In full scaling, by what factor drain current is scaled? (if S is the scaling factor)
Option A:	S
Option B:	1/S
Option C:	$1/S^2$
Option D:	S^2

Q22.	In Si process technology two metal layers can be joined by using-
Option A:	contact cut
Option B:	Wire
Option C:	Via
Option D:	Glass
Q23.	Which has better noise margins?
Option A:	nMOS
Option B:	pMOS
Option C:	CMOS
Option D:	BiCMOS
Q24.	Identify the invalid statement from the following statements-
Option A:	Separation from contact cut to transistor has to be 2λ
Option B:	Separation from implant to another transistor has to be 1λ
Option C:	Polysilicon to extend a minimum of 2λ beyond diffusion boundaries.
Option D:	Separation between multiple cuts is 2λ
Q25.	In full scaling which entity remains unchanged?
Option A:	Power density
Option B:	Power dissipation
Option C:	Current density
Option D:	Drain current

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0910_R16_BM_VII_BMC702_AK4

Question	Correct Option (Enter either 'A' or 'B' or 'C' or 'D')
Q1.	D
Q2.	A
Q3.	D
Q4	A
Q5	C
Q6	A
Q7	C
Q8.	A
Q9.	B
Q10.	B
Q11.	B
Q12.	A
Q13.	B
Q14.	D
Q15.	B
Q16.	A
Q17.	B
Q18.	A
Q19.	A
Q20.	C
Q21.	B
Q22.	C
Q23.	C
Q24.	B
Q25.	A