University of Mumbai

Examination 2020 under cluster 4 (PCE)

Program: BE Electronics and Telecommunication Engineering
Curriculum Scheme: Rev2012
Examination: Third Year Semester VI
Course Code: ETC606 and Course Name: _VLSI Design___
Time: 1 hour Max. Marks: 50

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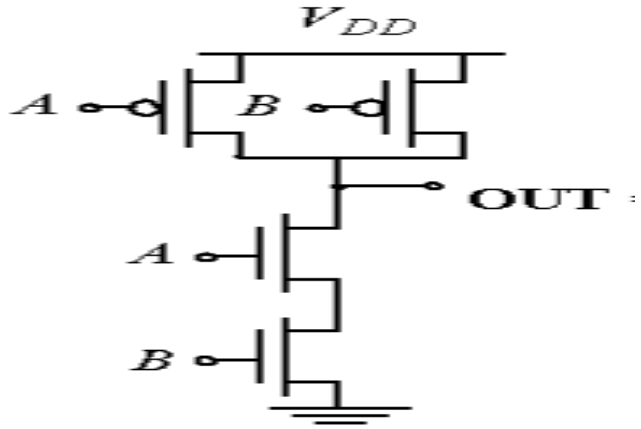
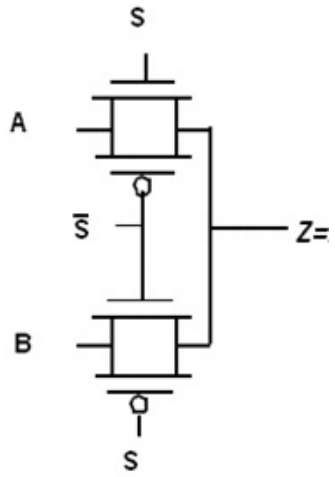
Note to the students:- All the Questions are compulsory and carry equal marks .

Q1.	The _____ is used to reduce the resistivity of poly silicon.
Option A:	Photo resist
Option B:	Etching
Option C:	Doping impurities
Option D:	Oxidation
Q2.	To grow the polysilicon gate layer, which of the following chemical is used for chemical vapour deposition?
Option A:	Silicon Nitride(Si3N4)
Option B:	Silane gas(SiH4)
Option C:	Silicon oxide
Option D:	Silicon dioxide
Q3.	As the channel length is reduced in a MOS transistor, depletion region width must be
Option A:	Increased
Option B:	Decreased
Option C:	Must not vary
Option D:	Exponentially decreased
Q4.	The size of a transistor is usually defined in terms of its
Option A:	Channel length
Option B:	Feature size
Option C:	Width
Option D:	Thickness ‘d’
Q5.	Which gives scalable design rules?
Option A:	Lambda rules
Option B:	Micron rules
Option C:	Layer rules
Option D:	Thickness rules
Q6.	What can be used for connecting Diffusion and polysilicon layers?
Option A:	Butting contact
Option B:	Buried contact
Option C:	Separate contact
Option D:	Cannot be connected
Q7.	What is minimum feature size for thick oxide?

Option A:	2λ
Option B:	3λ
Option C:	4λ
Option D:	λ
Q8.	The area of CMOS inverter is proportional to, which of the following?
Option A:	Area of n device
Option B:	Area of p device
Option C:	Total area of n and p device
Option D:	Square of minimum feature size
Q9.	The average power dissipated in resistive load n-MOS inverter is:
Option A:	0
Option B:	V_{DD} (V_{DD}-V_{OL})/R
Option C:	V_{DD} (V_{DD}-V_{OL})/2R
Option D:	V_{DD} (V_{DD}-V_{IH})/2R
Q10.	 For given circuit OUT =?
Option A:	AND gate
Option B:	NAND gate
Option C:	OR gate
Option D:	NOR gate
Q11.	Zipper logic style is
Option A:	Static CMOS
Option B:	Dynamic CMOS logic
Option C:	NORA Logic style
Option D:	C^2MOS logic style
Q12.	Advantages Dynamic CMOS Circuit over a Static CMOS Circuit
Option A:	Transistors required are more
Option B:	Transistors required are less
Option C:	Clock is not required
Option D:	Area required is more

Q13.	 For given circuit Z=?
Option A:	$Z = BS + A\bar{S}$
Option B:	$Z = AS + B\bar{S}$
Option C:	$Z = \bar{B}\,S + A\bar{S}$
Option D:	$Z = \bar{A}S + B\bar{S}$
Q14.	In clocked CMOS logic, rise time and fall time are
Option A:	Faster
Option B:	Slower
Option C:	Faster first and then slows down
Option D:	Flower first and then speeds up
Q15.	Read operation in memory is carried out using
Option A:	Sensor
Option B:	Decoder
Option C:	Amplifier
Option D:	Sense amplifier
Q16.	A full CMOS SRAM cell has
Option A:	8T
Option B:	6T
Option C:	4T
Option D:	2T
Q17.	1-bit DRAM is made of
Option A:	1-Flip-Flop
Option B:	1-Transistor and Capacitor
Option C:	1-Transistor
Option D:	1-Inverter
Q18.	In CMOS SRAM static power dissipation is low due to
Option A:	Moderate leakage current
Option B:	Large leakage current
Option C:	Small leakage current
Option D:	No leakage current

Q19.	What are carry generate combinations?
Option A:	If all the input are same then a carry is generated
Option B:	If all of the output are independent of the inputs
Option C:	If all of the input are dependent on the output
Option D:	If all of the output are dependent on the input
Q20.	A D flip-flop is used in a 4-bit serial adder, why?
Option A:	It is used to invert the input of the full adder
Option B:	It is used to store the output of the full adder
Option C:	It is used to store the carry output of the full adder
Option D:	It is used to store the sum output of the full addeR
Q21.	Based on how binary information is entered or shifted out, shift registers are classified into _____ categories.
Option A:	2
Option B:	3
Option C:	4
Option D:	5
Q22.	What is meant by parallel load of a shift register?
Option A:	All FFs are preset with data
Option B:	Each FF is loaded with data, one at a time
Option C:	Parallel shifting of data
Option D:	All FFs are set with data
Q23.	Power supply variation in the clock distribution causes a
Option A:	Jitter
Option B:	Skew
Option C:	Slack
Option D:	ESD
Q24.	Setup time is the interval of data signal arrived---------- the clock pulse
Option A:	Exact tick of
Option B:	Before
Option C:	After
Option D:	Delayed to
Q25.	The delay for a gate to switch 50% of its final if source resistance of 10kohm with the total lumped capacitance for a wire is 11pF
Option A:	242ns
Option B:	76ns
Option C:	110ns
Option D:	55ns

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Question	Correct Option (Enter either 'A' or 'B' or 'C' or 'D')
Q1.	C
Q2.	B
Q3.	B
Q4	A
Q5	A
Q6	A
Q7	B
Q8.	C
Q9.	C
Q10.	B
Q11.	B
Q12.	B
Q13.	B
Q14.	B
Q15.	D
Q16.	B
Q17.	B
Q18.	C
Q19.	B
Q20.	C
Q21.	C
Q22.	B
Q23.	A
Q24.	B
Q25.	B