University of Mumbai

Examination 2020 under cluster 4 (PCE)

Program: BE Electronics & Telecommunication Engineering
Curriculum Scheme: Rev2016
Examination: Third Year Semester VI
Course Code: ECCDLO6021 and Course Name: Digital VLSI design
Time: 1 hour Max. Marks: 50
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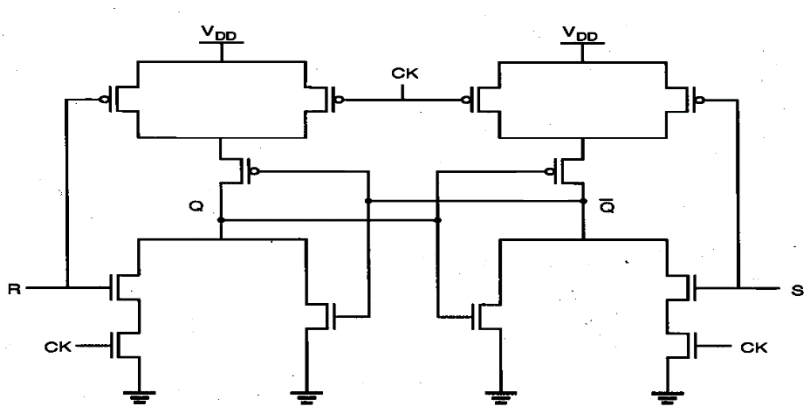
Note to the students:- All the Questions are compulsory and carry equal marks.

Q1.	What will be the output, When both nMOS and pMOS transistors of CMOS logic design are in OFF condition ?
Option A:	1 or Vdd or HIGH state
Option B:	0 or ground or LOW state
Option C:	High impedance or floating(Z)
Option D:	Crowbarred or Contention(X)
Q2.	Which region n transistor operates in Pseudo-nMOS logic ?
Option A:	cut off region
Option B:	saturation region
Option C:	resistive region
Option D:	non saturation region
Q3.	Which memory is volatile?
Option A:	PROM
Option B:	SRAM
Option C:	ROM
Option D:	PROM
Q4.	A full CMOS SRAM cell has
Option A:	8T
Option B:	6T
Option C:	4T
Option D:	2T
Q5.	Based on how binary information is entered or shifted out, shift registers are classified into _____ categories.
Option A:	2-Two
Option B:	3-Three
Option C:	4- Four
Option D:	5- Five

Q6.	In the adder, sum is stored in
Option A:	series
Option B:	cascade
Option C:	parallel
Option D:	registers
Q7.	Scaling a supply voltage helps to reduced
Option A:	Crosstalk
Option B:	Power
Option C:	Delay
Option D:	Speed
Q8.	Power supply variation in the clock distribution causes a _____
Option A:	Jitter
Option B:	Skew
Option C:	Slack
Option D:	ESD
Q9.	In FPGA, vertical and horizontal directions are separated by _____
Option A:	A line
Option B:	A channel
Option C:	A strobe
Option D:	A flipflop
Q10.	A PLA is similar to a ROM in concept except that
Option A:	It hasn’t capability to read only
Option B:	It hasn’t capability to read or write operation
Option C:	It doesn’t provide full decoding to the variables
Option D:	It hasn’t capability to write only
Q11.	Which of the following doesn't belongs to RTL design method?
Option A:	Capture the HLSM
Option B:	Create and connect data path to controller
Option C:	Derive the controller's FSM
Option D:	Disconnecting all controller Inputs and outputs

Q12.	It is not possible to use range with _____ types in VHDL
Option A:	Integer
Option B:	BIT_VECTOR
Option C:	STD_LOGIC
Option D:	Natural
Q13.	Which of the following HDLs are IEEE standard
Option A:	VHDL and Verilog
Option B:	C and C++
Option C:	Altera and XILINX
Option D:	Quartus and Maxplus II
Q14.	For realization of given expression Z=Bar(A+BC) means Z= $\overline{A+BC}$ using Pseudo N-mos design style, how many numbers of nMOS and pMOS transistors required respectively?
Option A:	nMOS=3 and pMOS=1
Option B:	nMOS=3 and pMOS=3
Option C:	nMOS=1 and pMOS=3
Option D:	nMOS=1 and pMOS=1
Q15.	In NOR type flash memory, each cell has one end is connected to
Option A:	Source
Option B:	Drain
Option C:	Gate
Option D:	Ground
Q16.	What is ripple carry adder?
Option A:	The carry output of the lower order stage is connected to the carry input of the next higher order stage
Option B:	The carry input of the lower order stage is connected to the carry output of the next higher order stage
Option C:	The carry output of the higher order stage is connected to the carry input of the next lower order stage
Option D:	The carry input of the higher order stage is connected to the carry output of the lower order stage

Q17.	A Barrel Shifter is a _____based digital circuit.
Option A:	Encoder
Option B:	Decoder
Option C:	Buffer
Option D:	Multiplexer
Q18.	ESD protection is carried out by using
Option A:	Transistor
Option B:	Clamping Diode
Option C:	Zener diode
Option D:	Diode
Q19.	PLA contains _____
Option A:	AND and OR arrays
Option B:	NAND and OR arrays
Option C:	NOT and AND arrays
Option D:	NOR and OR arrays
Q20.	Which of the following are common between HLSMs and FSMs?
Option A:	Transitions happen at the edge of a clock
Option B:	They have external complex data
Option C:	Transitions happen at the Level of a clock
Option D:	They don't have external complex data
Q21.	The circuit of the given figure is CMOS implementation of _____ 
Option A:	clocked NAND-based SR latch circuit.
Option B:	clocked NOR-based SR latch circuit.
Option C:	clocked XOR-based SR latch circuit.
Option D:	clocked XNOR-based SR latch circuit.

Q22.	In CMOS SRAM static power dissipation is low due to_____
Option A:	moderate leakage current
Option B:	large leakage current
Option C:	small leakage current
Option D:	no leakage current
Q23.	Adder using _____ technology can be used for speed improvement.
Option A:	CMOS
Option B:	BiCMOS
Option C:	nMOS
Option D:	pMOS
Q24.	Electrostatic discharge for 1pF and 1nC charge
Option A:	10kV
Option B:	1mV
Option C:	1kV
Option D:	10kV
Q25.	What is the advantage of using VHDL instead of any other HDL?
Option A:	Weak Typing
Option B:	Based on ADA
Option C:	Portability
Option D:	Easy to code

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Question	Correct Option (Enter either 'A' or 'B' or 'C' or 'D')
Q1.	C
Q2.	B
Q3.	B
Q4	B
Q5	C
Q6	C
Q7	A
Q8.	A
Q9.	B
Q10.	C
Q11.	D
Q12.	B
Q13.	A
Q14.	A
Q15.	D
Q16.	A
Q17.	D
Q18.	B
Q19.	A
Q20.	A
Q21.	B
Q22.	C
Q23.	B
Q24.	C
Q25.	C